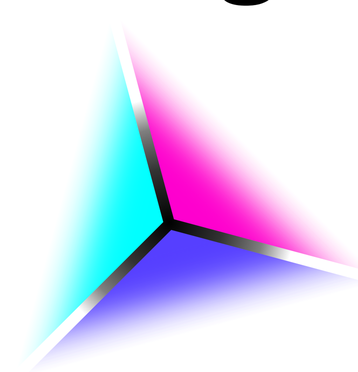
ICH01

Novel Gate Design Method for Short-Duration Test



Jan Bělohoubek

jan.belohoubek@fit.cvut.cz

CZECH TECHNICAL UNIVERSITY IN PRAGUE

Faculty of Information Technology

Abstract

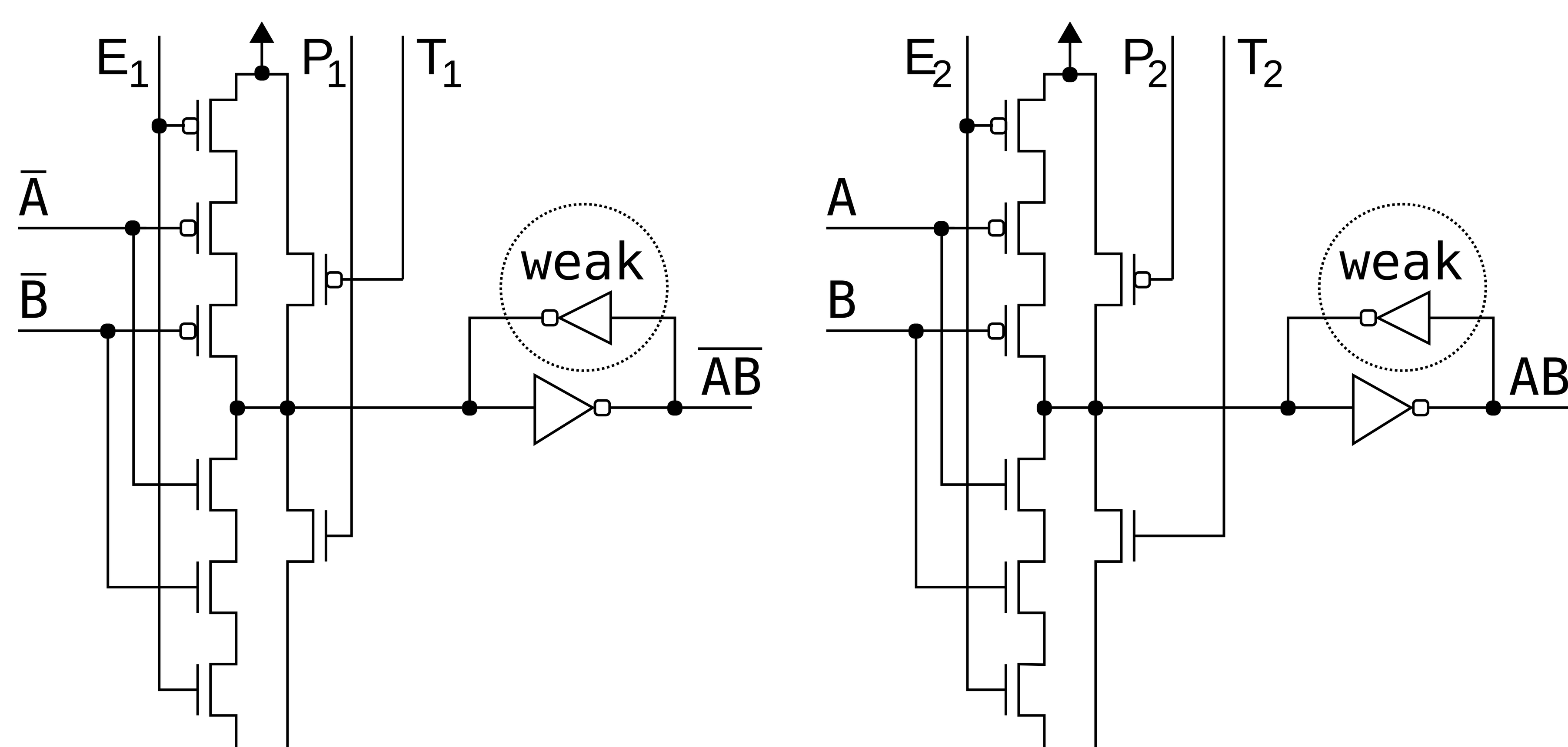
In this paper, a novel logic gate design method will be presented. This method allows to test combinational parts of the circuit using a short-duration offline test. Short-duration offline tests are usable when fault-recovery in duplex-based systems is required and downtime should be minimized at the same time. The presented method adopts some principles from dual-rail logic and asynchronous circuits design.

Stuck-at-fault model: observability and controlability

- Gate-level faults are considered
- Controlability and observability are very difficult tasks
  - Huge amount of test-vectors is required
  - Non-symmetric gates tend to propagate s@0 and s@1 faults differently

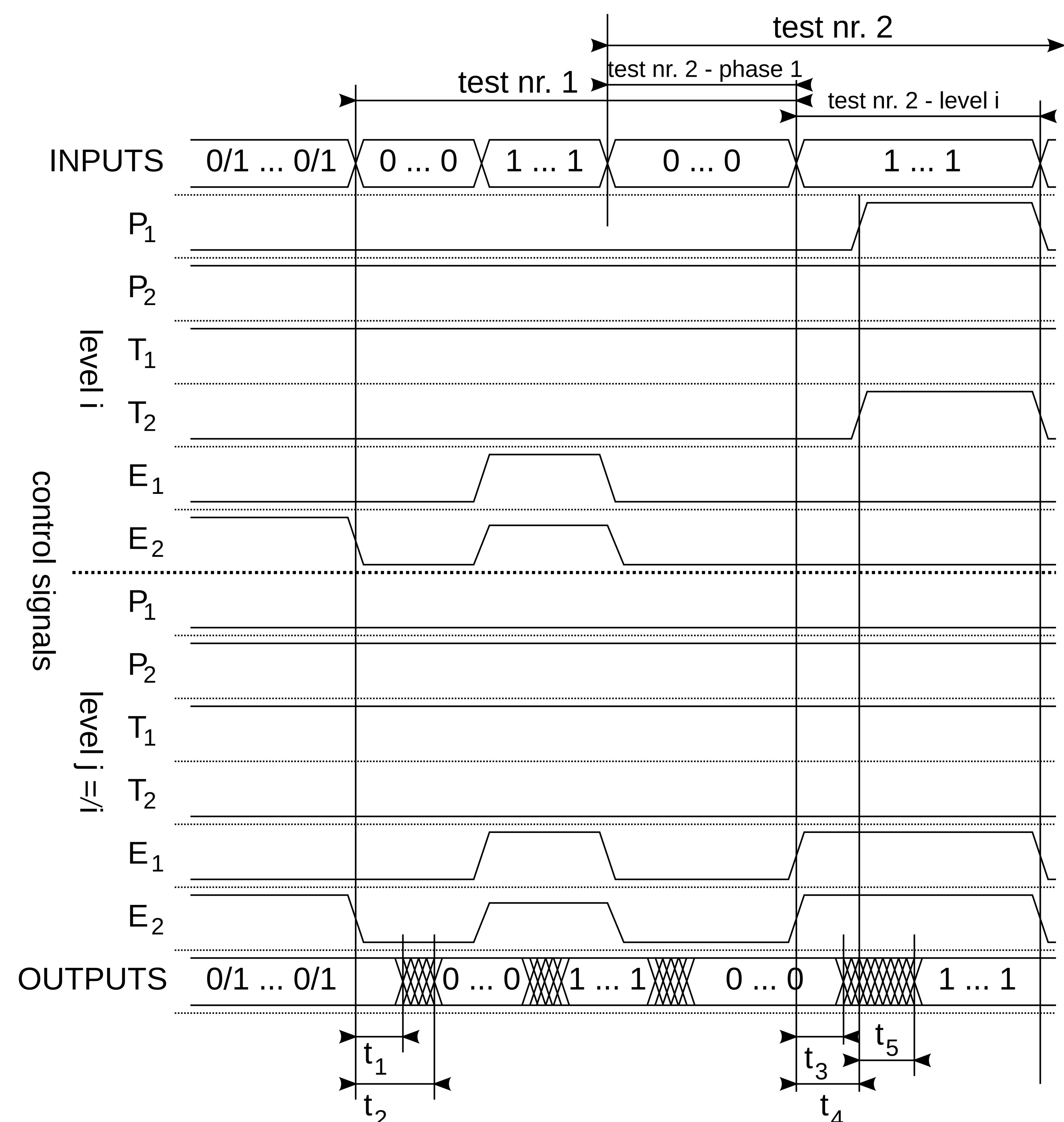
Proposed C-element-based gates

- Symmetric gates propagate all stuck-at-faults in the same way
- State-holding, generalized C-element-based structure implements a *monotonic gate* function
  - Proposed gates works in two phases: *Preset and Computation*
- Complete set of gates requires inverters
  - Dual-rail logic with complemetary signals is used
- Very simple test (all-zero and all-one) is used to discover all gate-level faults



Proposed dual-rail AND/NAND gate.

Proposed short-duration circuit test



- Proposed combinational logic test is sequential → fault presence is detected as the absence of the transition
  - The circuit is periodically flooded by zeros/ones
  - After the defined delay, the fault-free circuit output equals to the circuit input
  - The test length depends on the circuit depth

Conclusions

- Generalized C-element structure allows to create symmetric monotonic gates
- Proposed test allows to discover all gate-level stuck-at-faults in circuits composed of proposed gates