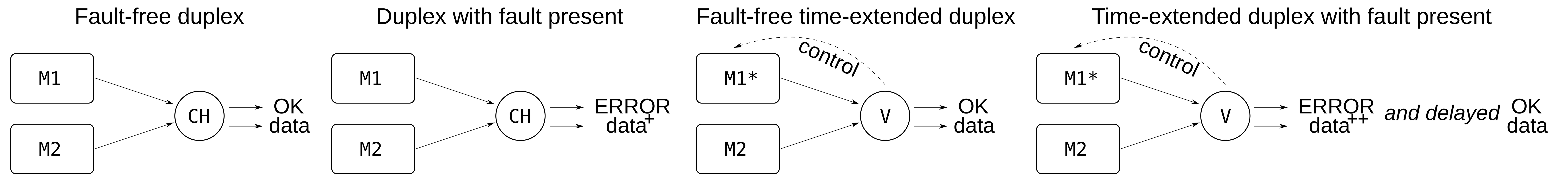
Novel C-Element-based Error Detection and Correction Method Combining Time and Area Redundancy

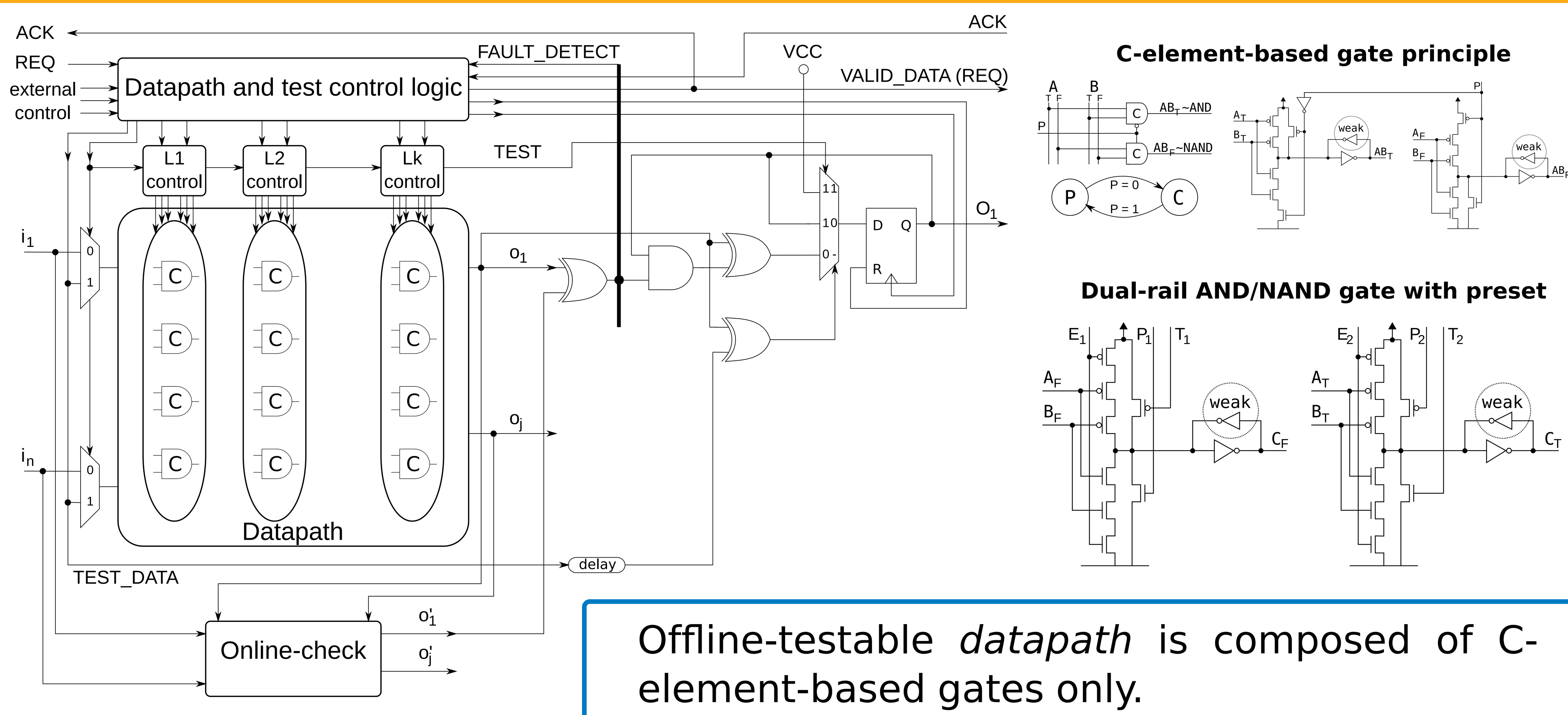
Introduction

- a novel fault-tolerant circuits design method with reduced area overhead
- a combination of **time and area redundancy**
- target architecture: the **time-extended duplex** scheme
  - → complete stuck-at fault testability by an **universal short-duration offline test** allowed by **new logic gate design**
  - → **allows to tolerate all** permanent, transient, and intermittent **stuck-at faults**



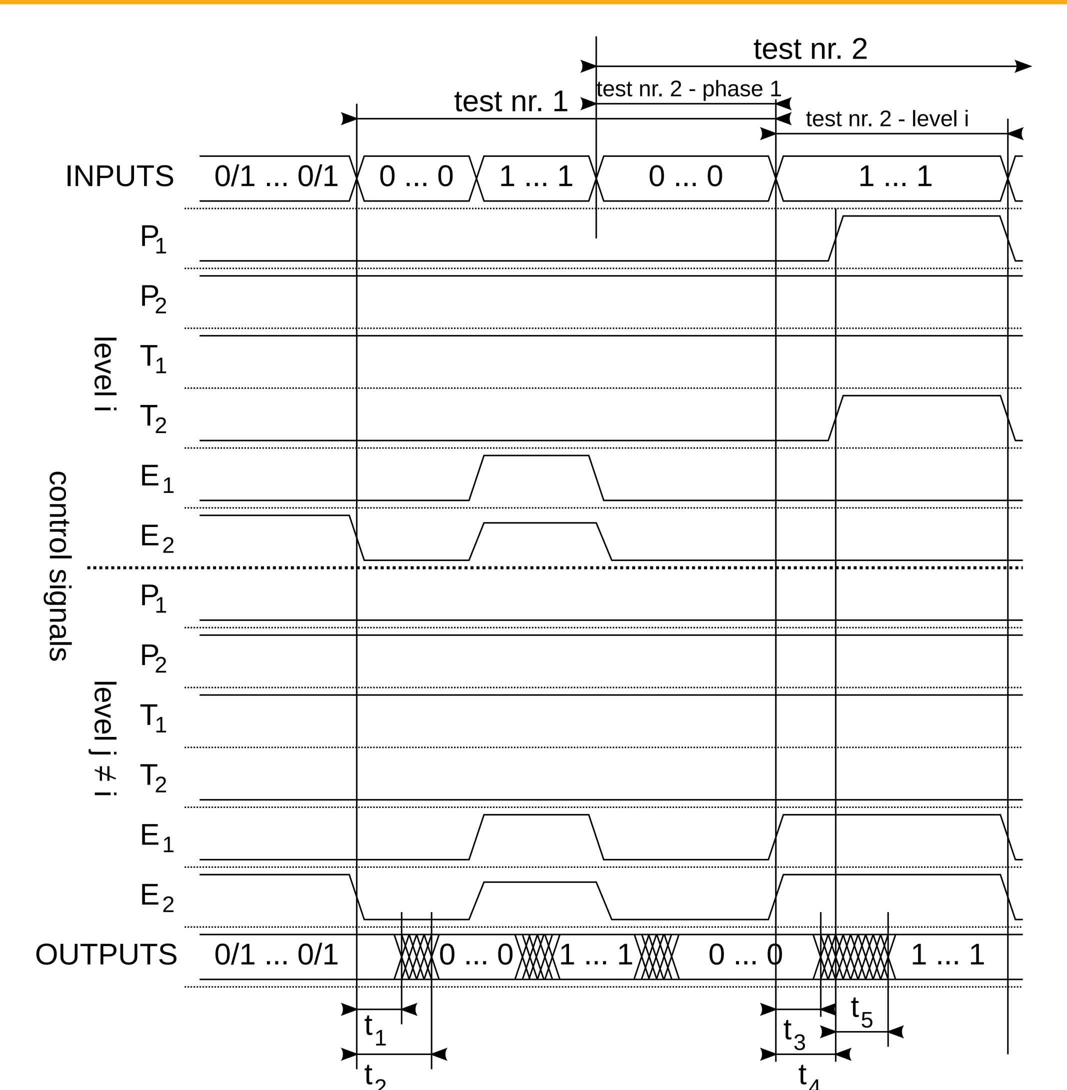
Permanent faults consequences are corrected using an universal short-duration offline test and transient faults are eliminated by recomputation.

Proposed architecture of the time-extended duplex scheme



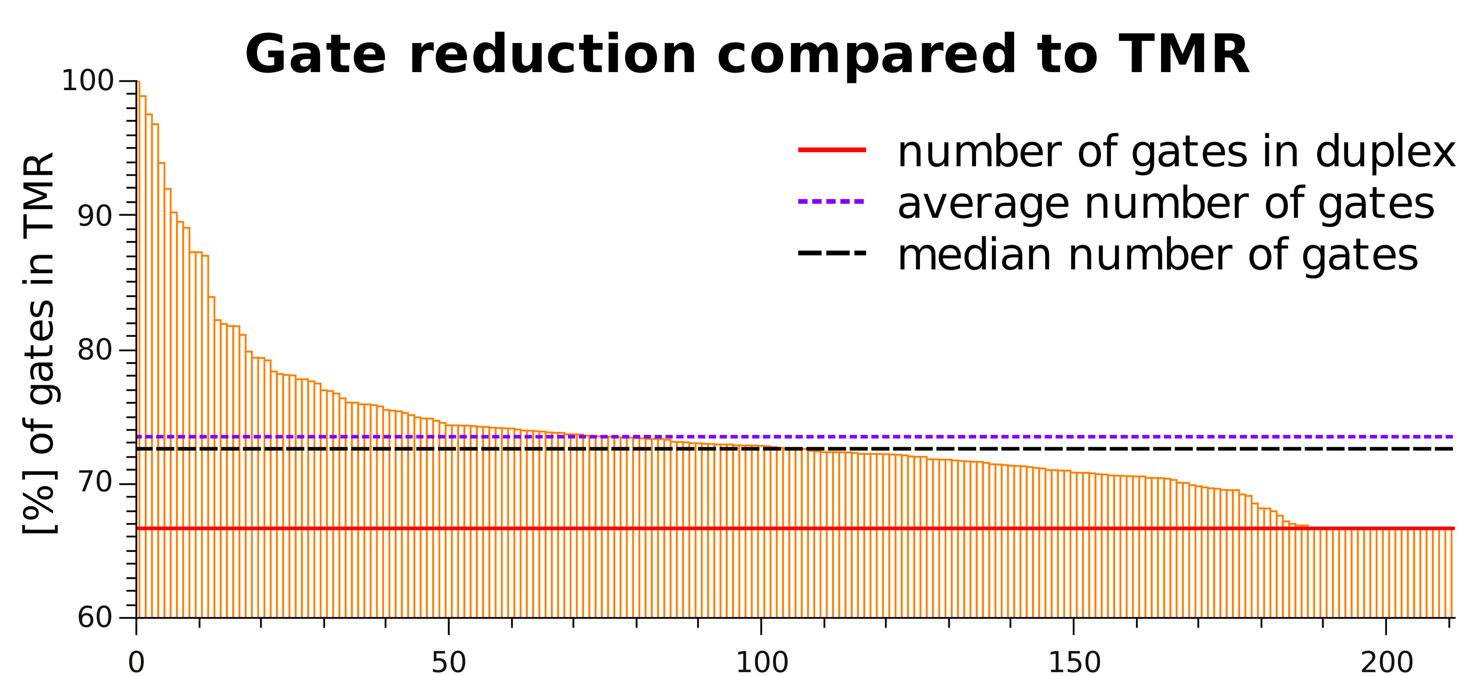
Offline-testable *datapath* is composed of C-element-based gates only.

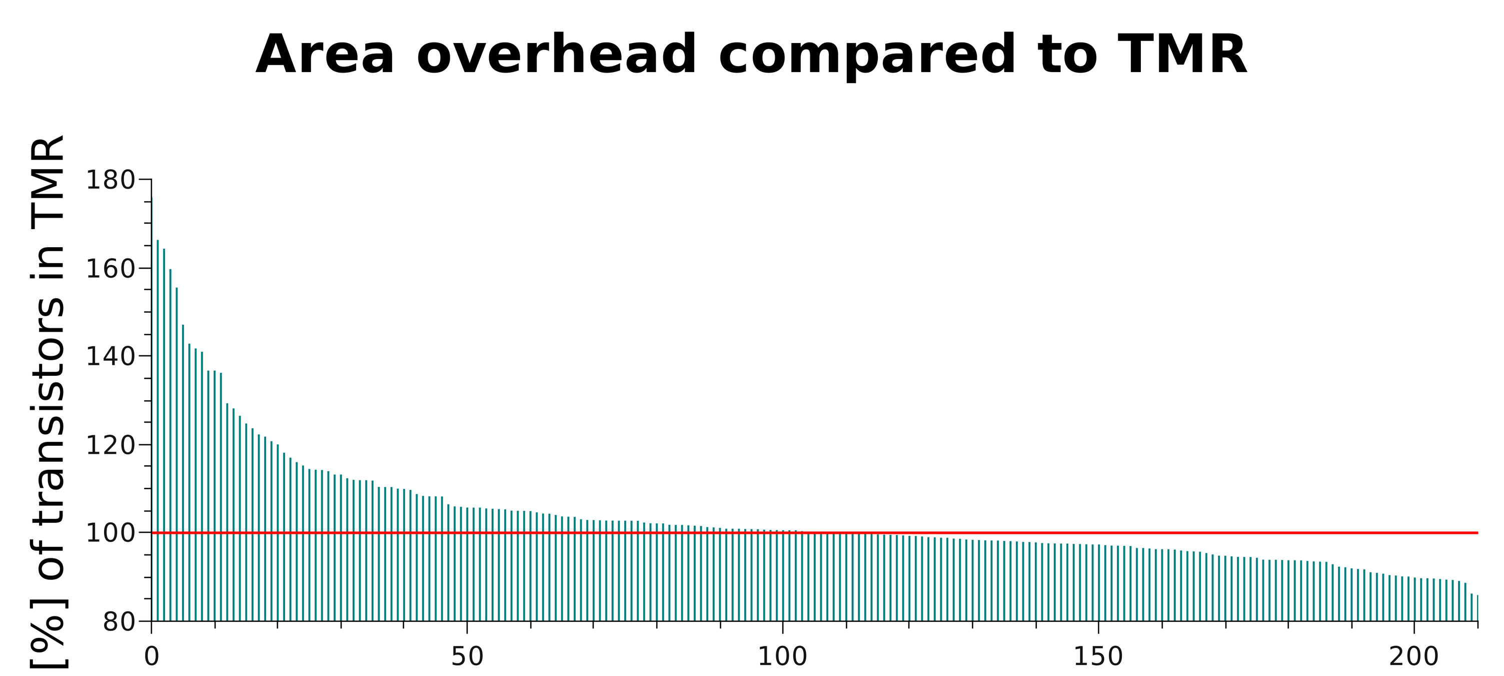
Proposed test



The short-duration offline test principle: **the combinational circuit is** periodically **flooded by zeros/ones** during the proposed combinational logic test. The test is sequential → **fault presence is** detected as the **absence of the transition**.

Preliminary results





Even though the number of gates in time-extended duplex is less than twice the number of gates in TMR, the real overhead is greater, because the proposed gates are larger. The results are related to two-input gates-based circuits.

Conclusions

- the **time-extended duplex scheme** is proposed
- a special gate design allowing an universal **short-duration offline test** is presented
- a complete stuck-at fault coverage was achieved
- **our method reduces the number of gates** compared to TMR **significantly**
- **significant savings** in transistors count **can be achieved** if the average gate fan-in will be increased
- **the main disadvantage is** that **the switching activity** rises exponentially when the number of ones and the number of zeroes is not balanced in input vectors

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