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Error Correction Method Based On The Short-Duration Offline Test

Jan Bělohoubek, Petr Fišer, Jan Schmidt

{jan.belohoubek, petr.fiser, jan.schmidt}@fit.cvut.cz

Czech Technical University in Prague
Prague, Czech Republic

DSD 2016, Limassol – Cyprus

Motivation

- What?
  - Combine time and area redundancy to achieve error-correction
  - Reduce the number of required test vectors from thousands to tens
- Why?
  - To reduce the total system costs
  - To reduce the test time and the test-hardware complexity
- How?
  - Employ an extremely short offline test – *short-duration offline test*
  - Describe the circuit properties required for the short-duration test
  - Propose special hardware structures enabling the short-duration test

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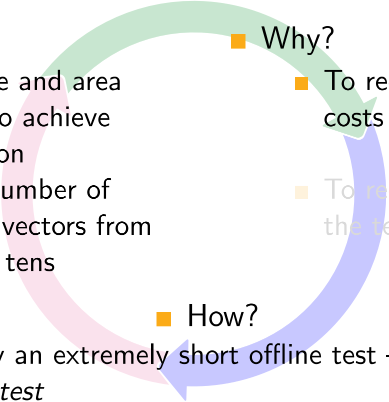

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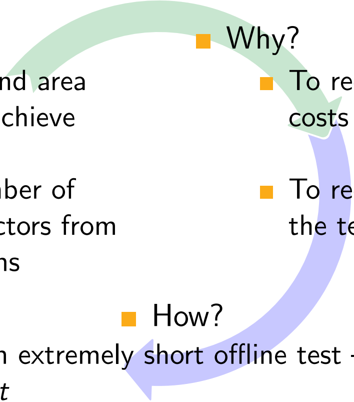

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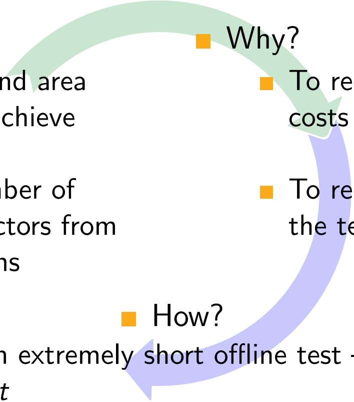

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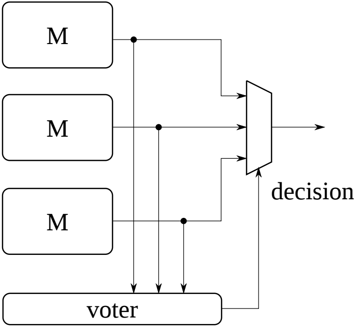
Fundamental Ideas
Error-Correction

- The most popular solution – TMR



Fundamental Ideas

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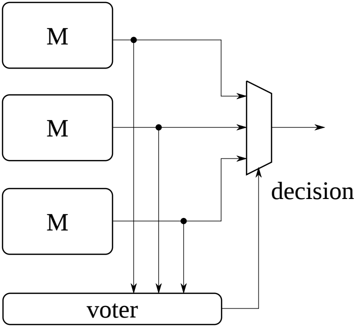
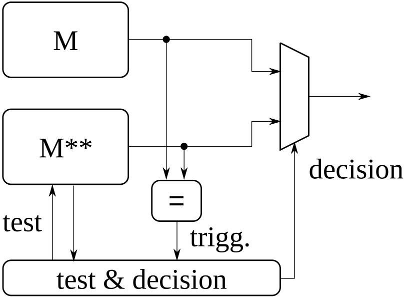


- The proposed solution – *Time-Extended Duplex* (TED)



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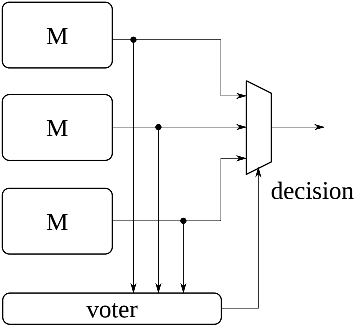

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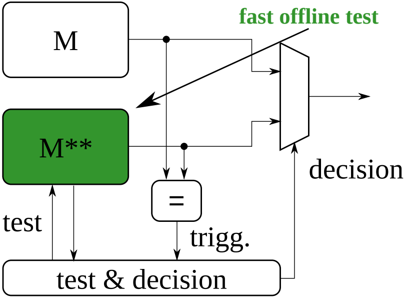
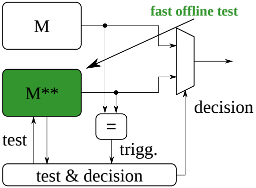


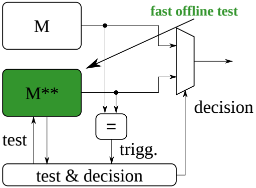
Fundamental Ideas

Short-Duration Offline Test



What is required:

Fundamental Ideas
Short-Duration Offline Test



What is required:

- the test length in orders of tens of computational (clock) cycles only

Fundamental Ideas
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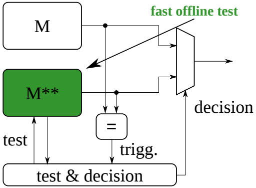

What is required:

- the test length in orders of tens of computational (clock) cycles only
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Fundamental Ideas
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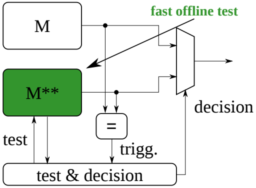

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→ *short-duration offline test*

Fundamental Ideas
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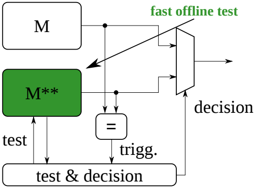

What is required:

- the test length in orders of tens of computational (clock) cycles only
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→ *short-duration offline test*

→ *special hardware structures*

Observation

Stuck-At-Fault Model

- Only two test vectors are required to achieve 100% fault-coverage: *all-zero* and *all-one* vector

Theorem

There is a two-vector-testable class of circuits with respect to the stuck-at-fault model.

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Observation

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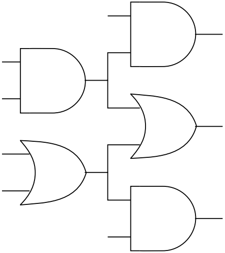

Required circuit properties:

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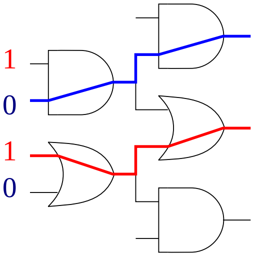

stuck-at-1 / fault symptom: 1

stuck-at-0 / fault symptom: 0

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→ Every stuck-at-fault is observable

Efficient Monotonic Circuit

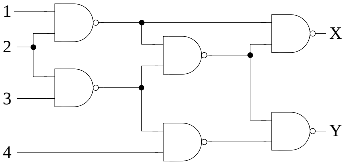
Circuit Transformation

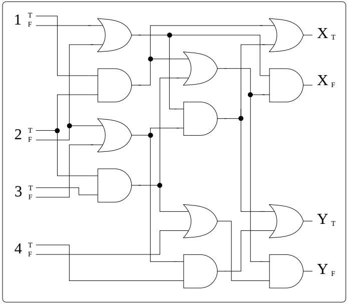
How to build the circuit complying with the “required properties”

- Make the circuit monotonic – employ *dual-rail logic*
- Reconfigurable gates – OR/AND gate
  - + less gates
  - + fault symptoms at the fault-affected wires
  - − reconfigurable gate OR/AND is complex

Efficient Monotonic Circuit

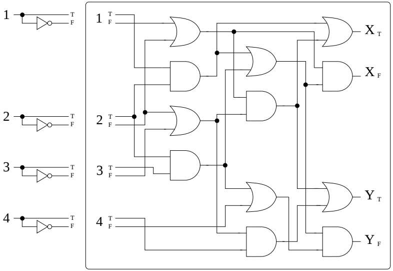
Dual-Rail Implementation





Efficient Monotonic Circuit

Dual-Rail Implementation



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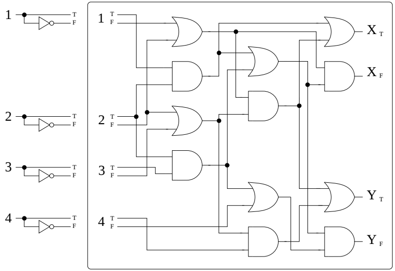
Efficient Monotonic Circuit
Dual-Rail Implementation



- If the dual-rail logic serves as the inverter replacement only, the number of gates can be reduced

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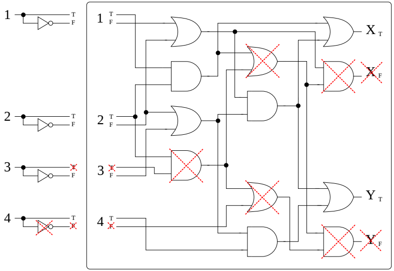
Efficient Monotonic Circuit

Dual-Rail Reduction



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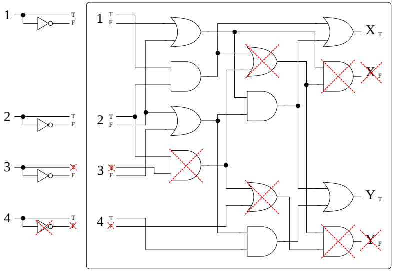
Efficient Monotonic Circuit

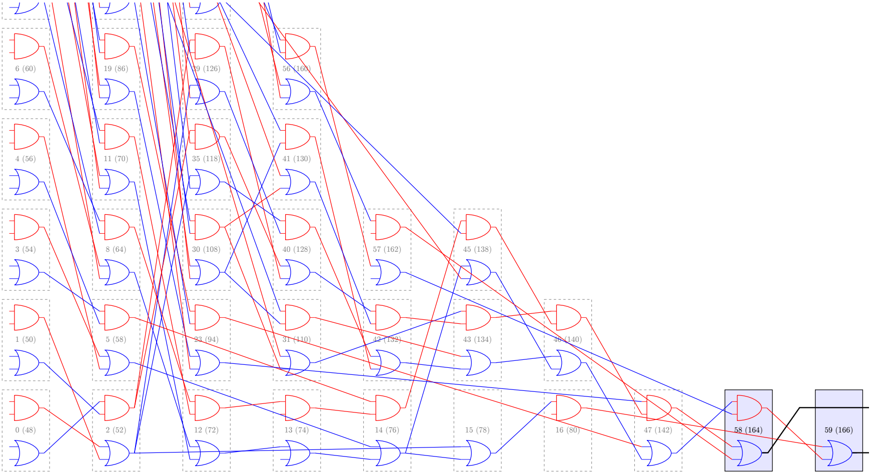
Dual-Rail Reduction



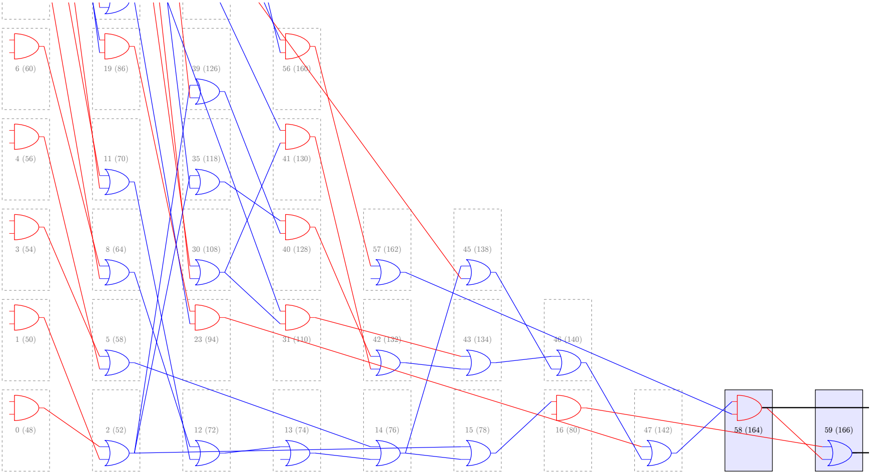
- If the dual-rail logic serves as the inverter replacement only, the number of gates can be reduced
- The number of gates can be the same as in the single-rail implementation (in the best case)
- Sometimes is the output polarity optional – this affects the *reduction success* → heuristics were developed

Dual-Rail Reduction

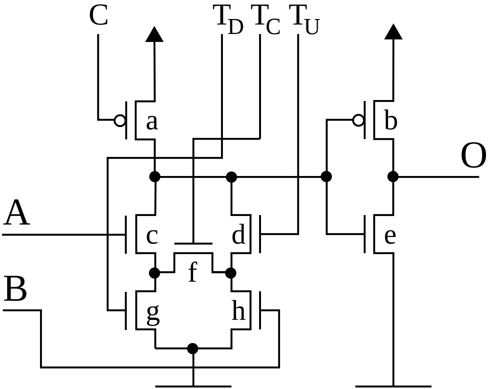
Positive outputs only (Cordic benchmark)



Dual-Rail Reduction
Greedy heuristic (Cordic benchmark)

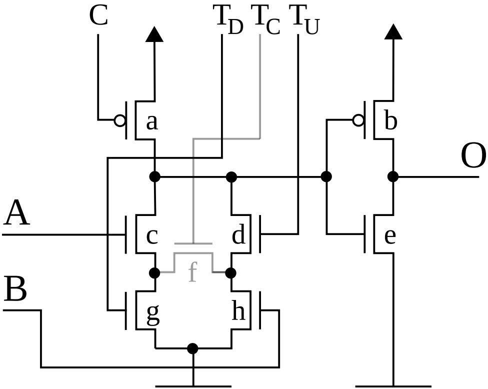


Reconfigurable Gate Design



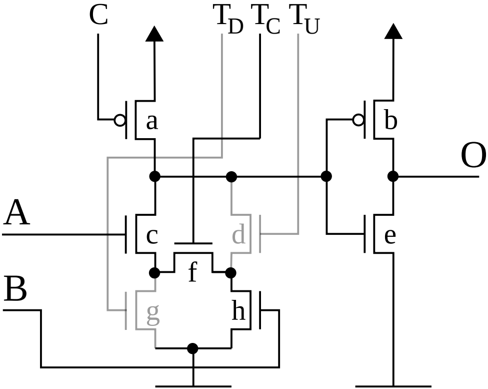
- Domino-logic AND/OR gate with increased controlability

Reconfigurable Gate Design



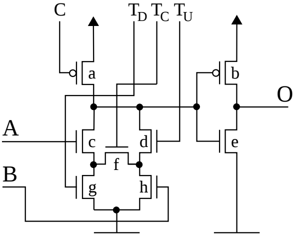
- Domino-logic OR gate $T_D = 1,\ T_C = 0,\ T_U = 1$

Reconfigurable Gate Design



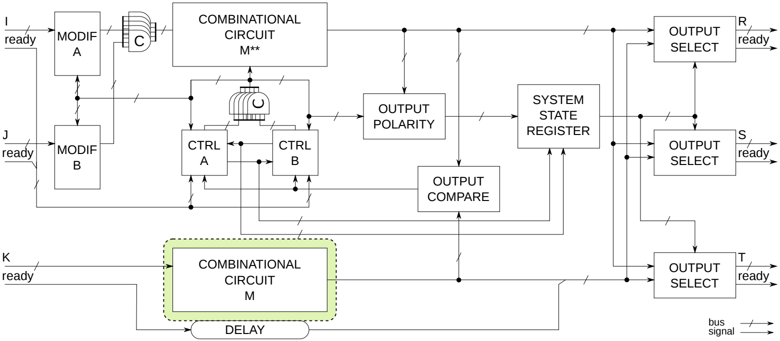
- Domino-logic AND gate $T_D = 0,\ T_C = 1,\ T_U = 0$

The Offline Test Overview



- Combinational logic test
- Test of the reconfiguration is required → longer test
- Inspired by two-vector-testability; uses the state-holding property and the increased controlability of dynamic gates
- Test of all *stuck-open*/*stuck-on* faults
- The test length remains in orders of tens computational cycles only

Structure of the TED
Original Combinational Part



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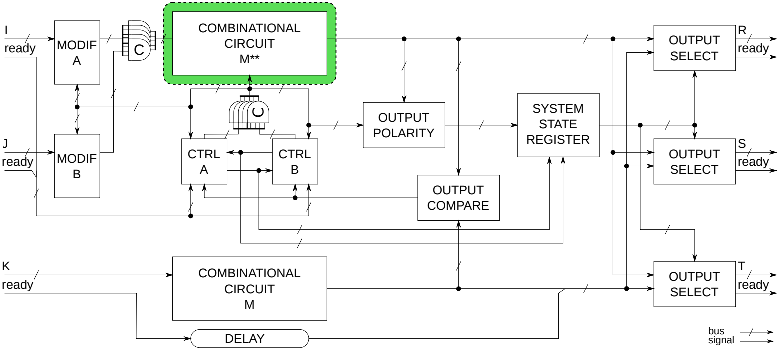
Structure of the TED

Offline-Testable Combinational Part



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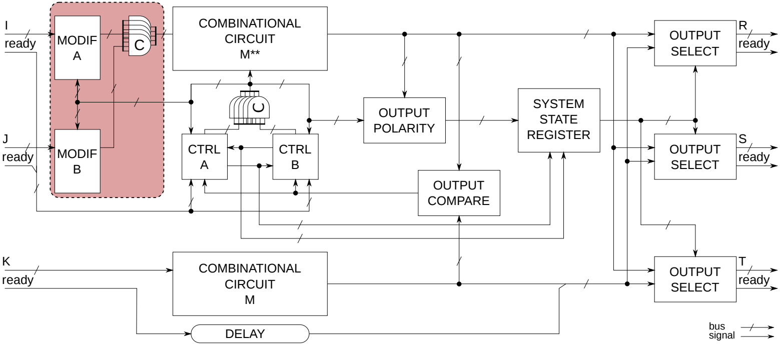
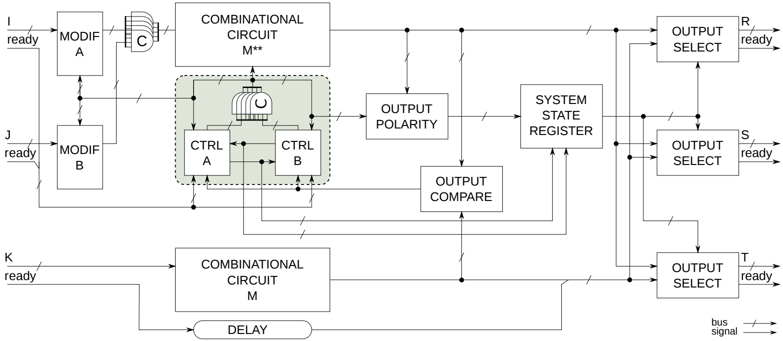
Structure of the TED
Single-Rail to Dual-Rail and Test Input Gen.



Structure of the TED
Test Control Part



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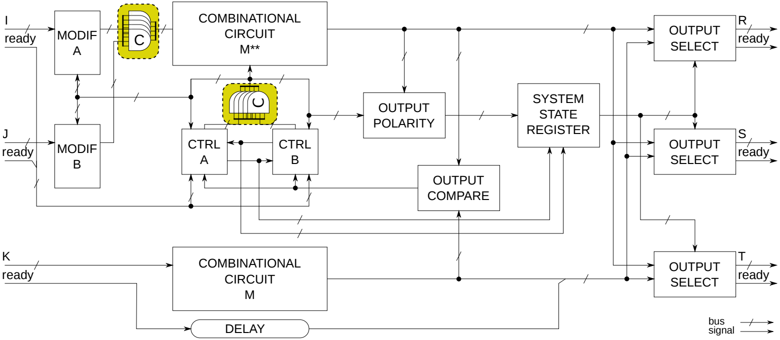
Structure of the TED

Duplex Checkers



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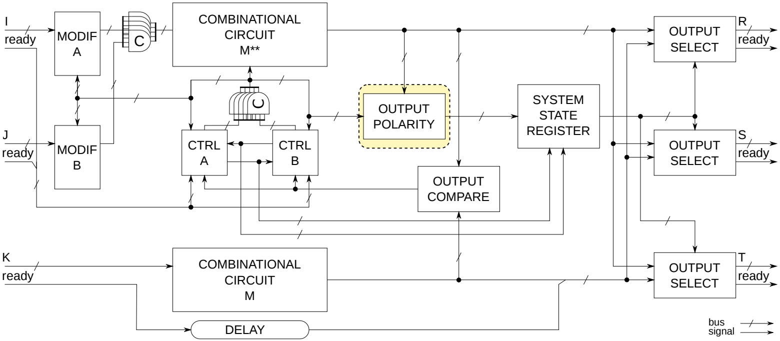
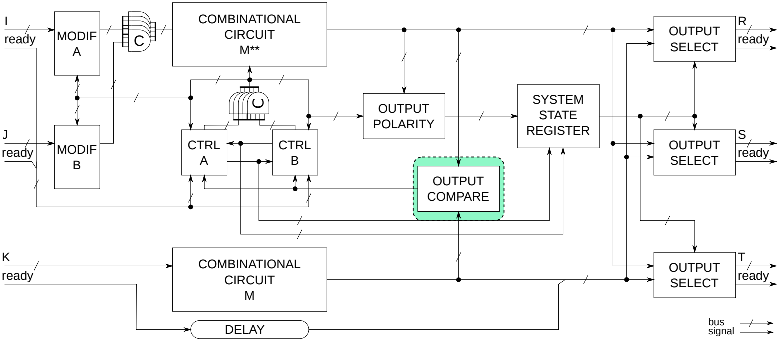
Structure of the TED

Test Response Evaluation



Structure of the TED

Test Trigger



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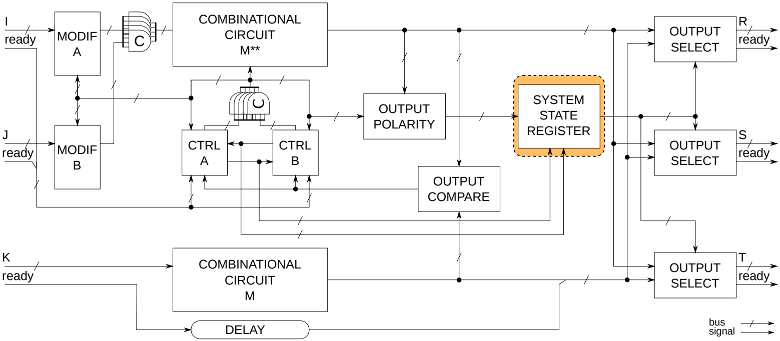
Structure of the TED
Last Test Results



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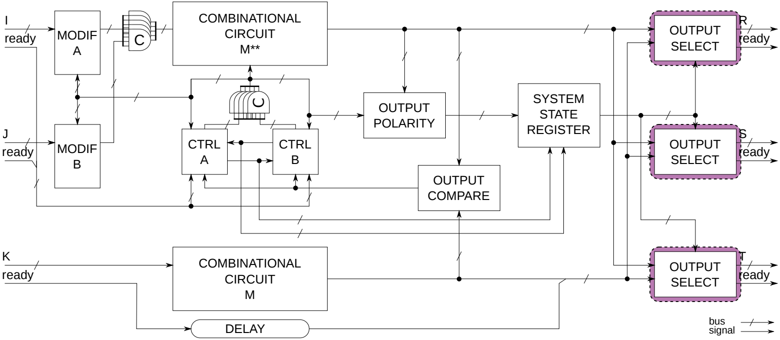
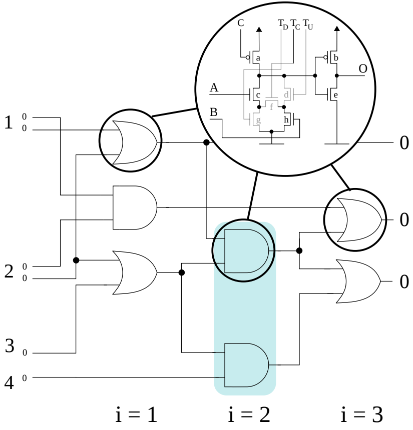
Structure of the TED

Corect Output Selection



Offline Test in Detail

Sub-Test 1 at Level 2



step	C	T_U	T_C	T_D	O
1	set circuit primary inputs to 0				
2	start at level $i = 1$				
3	at all levels:				
	0	0	0	0	↓
4	at level *i*:				0
	1	1	1	1	↑
5	at level *i*:				1
	1	0	0	0	1
6	at levels other than *i*:				0
	1	0	1	0	0
7	set circuit primary inputs to 1				↑
8	Check if the circuit output is *all-one*				1
9	if $(++\mathrm{i} \leq \mathrm{depth})$ then goto 3				1

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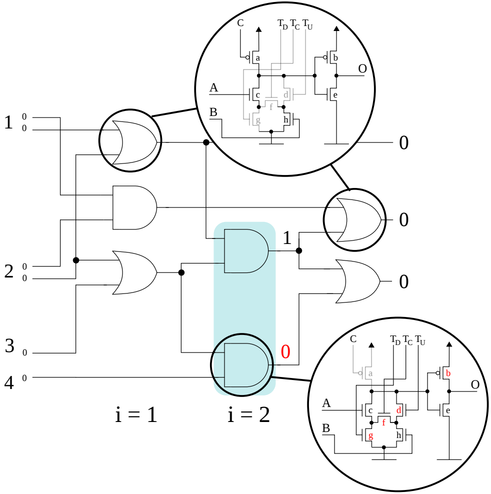

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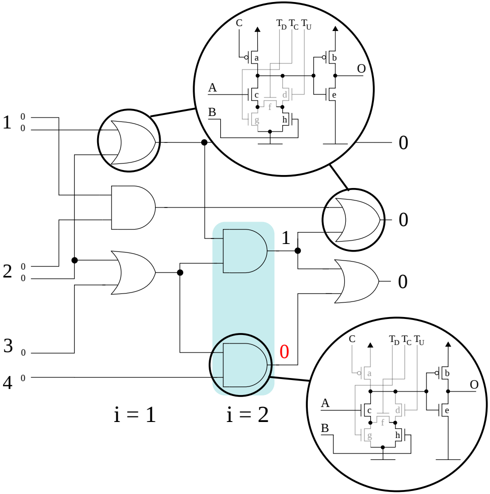

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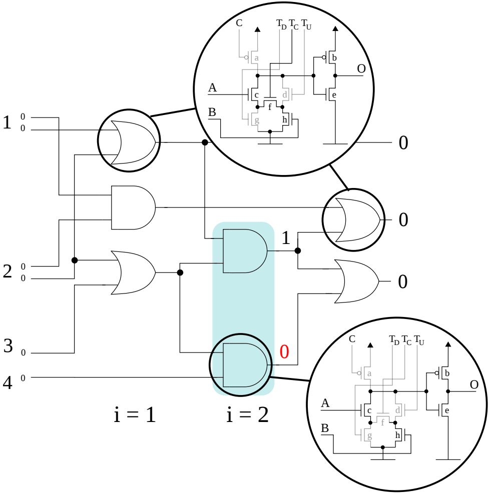

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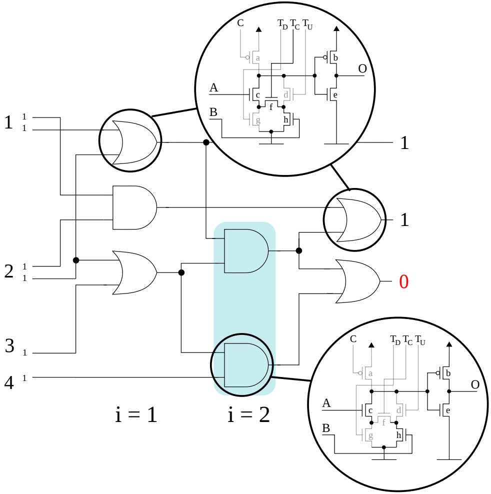
	0	0	0	0	↓
4	at level *i*:				0
	1	1	1	1	↑
5	at level *i*:				1
	1	0	0	0	1
6	at levels other than *i*:				0
	1	0	1	0	0
7	set circuit primary inputs to 1				↑
8	Check if the circuit output is *all-one*				1
9	if $(++i \leq \text{depth})$ then goto 3				1

Offline Test in Detail
Sub-Test 1 at Level 2



step	C	T_U	T_C	T_D	O
1	set circuit primary inputs to 0				
2	start at level $i = 1$				
3	at all levels:				
	0	0	0	0	↓
4	at level *i*:				0
	1	1	1	1	↑
5	at level *i*:				1
	1	0	0	0	1
6	at levels other than *i*:				0
	1	0	1	0	0
7	set circuit primary inputs to 1				↑
8	Check if the circuit output is *all-one*				1
9	if $(++i \leq \text{depth})$ then goto 3				1

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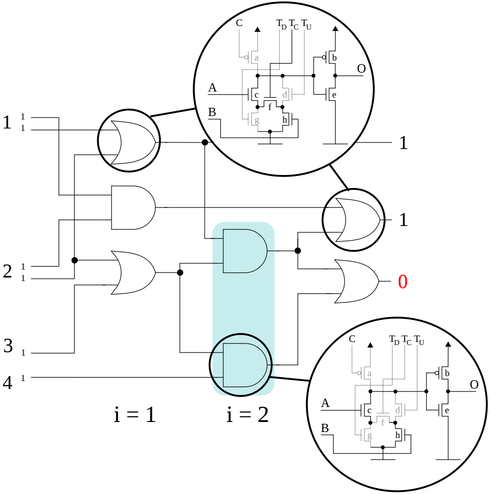
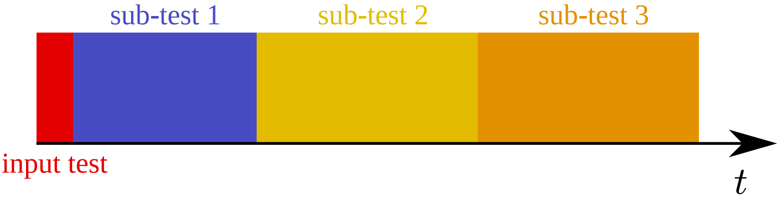
Offline Test in Detail
Sub-Test 1 at Level 2



step	C	T_U	T_C	T_D	O
1	set circuit primary inputs to 0				
2	start at level $i = 1$				
3	at all levels:				
	0	0	0	0	↓
4	at level *i*:				0
	1	1	1	1	↑
5	at level *i*:				1
	1	0	0	0	1
6	at levels other than *i*:				0
	1	0	1	0	0
7	set circuit primary inputs to 1				↑
8	Check if the circuit output is *all-one*				1
9	if (++i ≤ depth) then goto 3				1

The Offline Test Length



$$(2t_e) + (dt_e) + (t_e + dt_e) + (t_e + dt_e)$$

$$t_{tot} \leq (3d + 4) \cdot t_e$$

- Classical test $>> 1000 \cdot t_e$
- Proposed test $< 100 \cdot t_e$

t_e – computational (clock) cycle time; d – circuit depth

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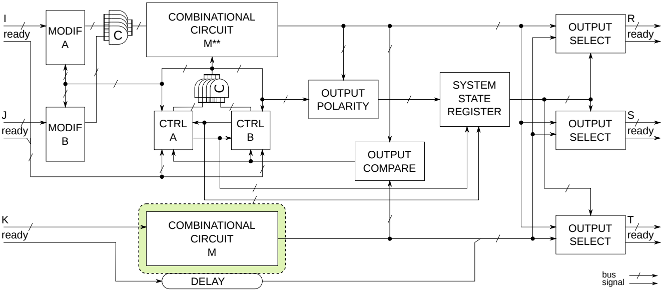
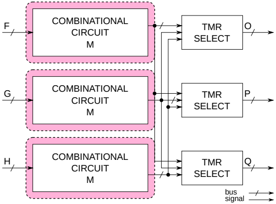
Comparison
TMR vs. TED





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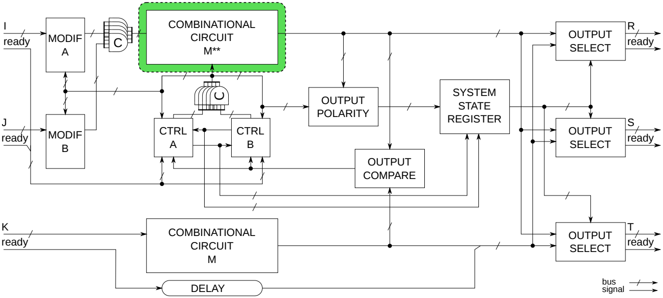
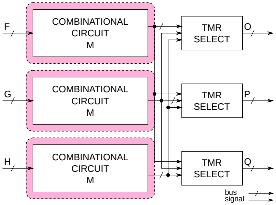
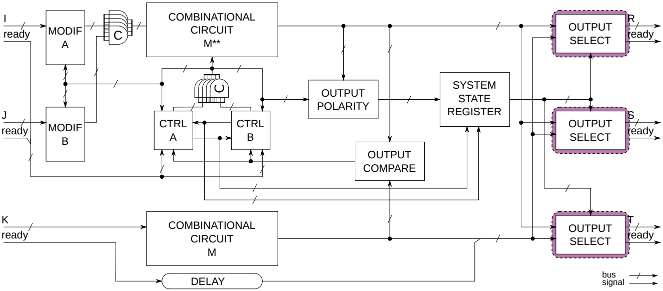
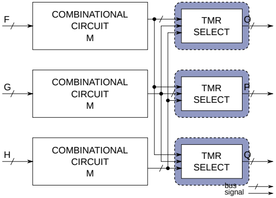
Comparison
TMR vs. TED



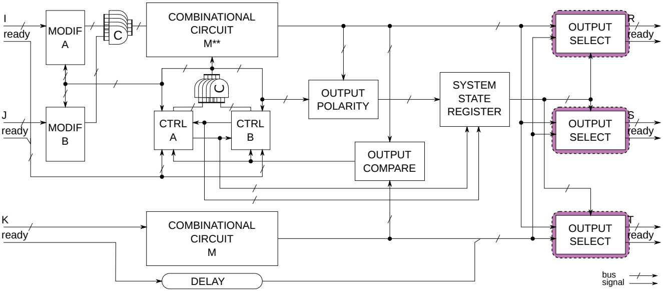


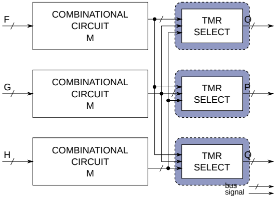
Comparison TMR vs. TED





Comparison
TMR vs. TED

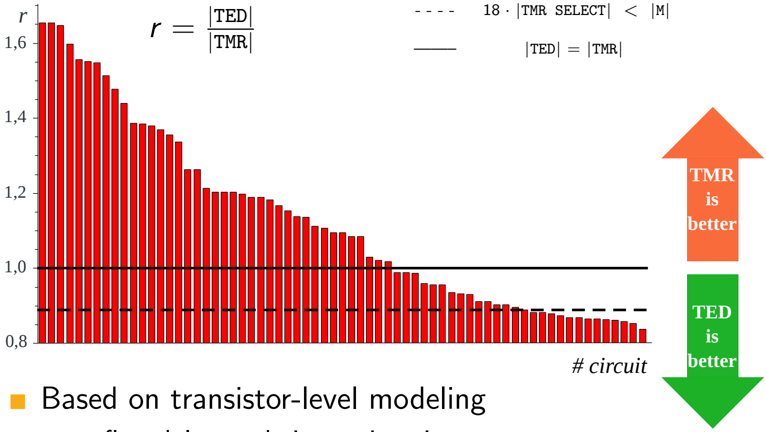




$$18 \cdot \left|\texttt{TMR SELECT}\right| \; < \; \left|\texttt{M}\right|$$

Comparison

Results (IWLS'2005 benchmark circuits)



$$r = \frac{|\mathtt{TED}|}{|\mathtt{TMR}|}$$

- Based on transistor-level modeling

  → fine delay and size estimation

- TED-friendly class of circuits has been identified

Thank you!

- The principle of the short-duration offline test was presented
- Novel gate structure allowing the offline test was introduced
- The novel error-correcting design method combining time and area redundancy was developed (TED)
- The efficient monotonic circuit implementation was presented
- Usage of the TED was suitable (compared to the TMR system) for circuits having relatively large combinational parts and small number of outputs

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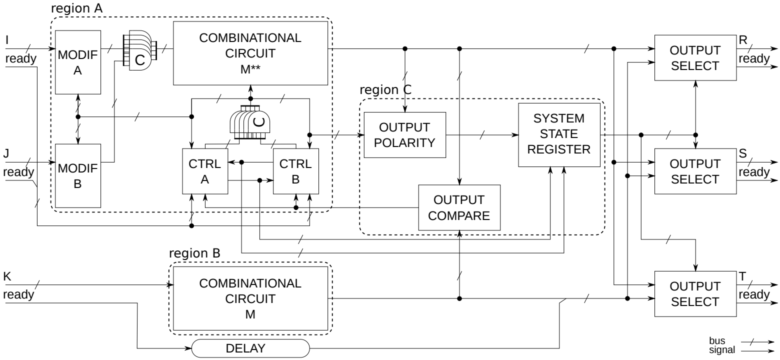
What happens when . . . ?



region A
I
ready
MODIF
A
C
COMBINATIONAL
CIRCUIT
M**
J
ready
MODIF
B
C
CTRL
A
CTRL
B
region C
OUTPUT
POLARITY
SYSTEM
STATE
REGISTER
OUTPUT
COMPARE
region B
K
ready
COMBINATIONAL
CIRCUIT
M
DELAY
OUTPUT
SELECT
R
ready
OUTPUT
SELECT
S
ready
OUTPUT
SELECT
T
ready
bus
signal